| | | | |
|---|---|---|---|
| Course unit title: | **Microprocessor Architecture** | | |
| Course unit code: | AEEE295 | | |
| Type of course unit: | Compulsory | | |
| Level of course unit: | Bachelor (1st Cycle) | | |
| Year of study: | 2 | | |
| Semester when the unit is delivered: | 4 | | |
| Number of ECTS credits allocated : | 6 | | |
| Name of lecturer(s): | Dr. Haris Haralambous | | |
| Learning outcomes of the course unit: | 1. Evaluate VLSI technology performance/cost/power consumption tradeoffs.<br>2. Describe the function of the pins and signals of the x86 family of processors and the loading and timing of the x86 microprocessors.<br>3. Design memory maps and Implement Address decoding circuits using NAND gates, comparators, decoder and NAND gate and programmable logic.<br>4. Perform memory timing analysis and synchronization using asynchronous buses and wait states and describe Isolated and memory mapped I/O.<br>5. Design Interfaces with two state devices such as LEDs, 7-segment displays, switches, keyboards relays and ac loads using buffers, latches and programmable I/O devices.<br>6. Write programs performing I/O synchronization using the polling technique. | | |
| Mode of delivery: | Face-to-face | | |
| Prerequisites: | AEEE191, AEEE195 | Co-requisites: | None |
| Recommended optional program components: | None | | |
| Course contents: | • **Introduction to microprocessors:** Overview of microprocessor technologies.<br>• **Introduction to the x86 family:** Pin and signal descriptions, loading and timing of the 80x86 microprocessors. Bus drivers, clock and reset circuits.<br>• **Memory interfacing, and synchronization:** Interfacing with EPROMs, Static and Dynamic RAMs. Address decoding, memory maps and memory mirroring. Static and dynamic bus contention. Memory timing analysis, synchronization using asynchronous buses and wait states.<br>• **Input/Output interfacing:** Isolated and memory mapped I/O. Interfacing with two state devices such as LEDs, 7-segment displays, switches, keyboards relays and ac loads. I/O synchronization using interrupts and the polling technique. Software and hardware aspects of interrupts. Use of programmable I/O devices.<br>• **Analog interfacing:** Digital to analog and analog to digital converters, operation, characteristics and interfacing. Synchronization between data converters and a microprocessor. Applications of data converters. | | |

| | |
|---|---|
| | • **Microcomputer Architecture:** Interfacing and programming of typical devices found in microcomputers such as Programmable Interface Adaptors (PIA, PIO),<br>• **Interrupts and DMA:** Programmable Interval Timers (PIT), Programmable Interrupt Controllers (PIC) and Direct Memory Access Controllers (DMAC), and USART. Computer bus standards. |
| Recommended and/or required reading: | |
| Textbooks: | B. Brey, *The Intel Microprocessors: 8086,80186,80286,80386, 80486, Pentium and Pentium Pro Processors, Pentium II, Pentium III and Pentium 4: Architecture, Programming and Interfacing*, Prentice Hall, 2003 |
| References: | J. P. Hayes, *Computer Architecture and Organization*, 3Ed, McGraw Hill., 2005 |
| Planned learning activities and teaching methods: | The taught part of course is delivered to the students by means of lectures, conducted with the help of computer presentations. Lecture notes and presentations are available through the web for students to use in combination with the textbooks. Lectures are supplemented with laboratory work carried out at the communications laboratory. During laboratory sessions, students perform individual or small group experiments performed with single board computers. Experiments include monitor commands, reset circuits, buffering, memory interfacing and I/O interfacing. |
| Assessment methods and criteria: | • Assignments 10%<br>• Tests: 20%<br>• Laboratory Work: 10%<br>• Final Exam 60% |
| Language of instruction: | English |
| Work placement(s): | No |