Course unit title:	Digital Integrated Circuits		
Course unit code:	AEEE438		
Type of course unit:	Compulsory		
Level of course unit:	Bachelor (1st Cycle)		
Year of study:	3		
Semester when the unit is delivered:	5 (Fall)		
Number of ECTS credits allocated :	6		
Name of lecturer(s):	Christos Themistos		
Learning outcomes of the course unit:	1. Analyse the various issues involved during the design of Digital Integrated Circuit such as the static power, dynamic power, propagation delay, noise margin, chip size. 2. Implement Logic Gates using Diode Logic and Diode Transistor Logic. 3. Explain the internal structure (in transistor level) and operation of the CMOS inverter and CMOS NAND and NOR gates. 4. Compare and argue the internal structure (in transistor level) and operation of the ECL inverter and ECL OR and NOR gates. 5. Compare and argue the internal structure (in transistor level) and operation of the TTL inverter and TTL NAND gates. 6. Design more advanced logic functions based on the knowledge of the basic inverter and NAND and NOR gates.		
Mode of delivery:	Face-to-face		
Prerequisites:	AEEE238	Co-requisites:	None
Recommended optional program components:	None		
Course contents:	**Characteristics of logic circuits**: Definition of digital logic design, noise margins, voltage and current characteristics, transient characteristics, rise time and fall time, noise immunity and loading, speed, power dissipation and levels of a logic inverter gate, propagation delay, power-delay product. **Diode Logic**: OR and AND diodel logice based gates, Diode Transistor Logic based NAND gate. **Transistor Transistor Logic (TTL), Complimentary and Emitter Coupled Logic (ECL):** Prototype and standard TTL Inverter, Internal Structure, Voltage and current logic operating levels, noise immunity, speed, power dissipation and levels of integration. Interconnecting logic families. ECL NOR –OR gate.		

	Metal Oxide Semiconductor (CMOS): Review of MOS transistor (nmos / pmos), current-voltage characteristics, capacitance. CMOS Inverter voltage transfer characteristics, noise margins, CMOS gate sizing, W/L aspect ratio. CMOS NOR and NAND gates. **VLSI Design:** basic layout, subsystem layout, and mask layout, CAD/CAE tools. **VLSI fabrication techniques**: Silicon Technology, Crystal growth through diffusion, ion implementation, oxidation, photolithography, metalization and packaging. **VLSI design examples**: CMOS Inverter.
Recommended and/or required reading:	
Textbooks:	Microelectronics Circuits, Adel Sendra and Kenneth Smith, Oxford University Press; 7 edition, 2014.
References:	1. Electronic Circuit Design, An Engineering approach, Savant Roden and Carpernter, Benjamin-Cummings Publishing co., 1987. 2. Digital Fundamentals, Floyd, Charles Merril Publishing co., 1986. 3. Microelectronic Circuit Analysis, Richard Jaeger, McGraw Hill co., 1997. 4. VLSI Techniques for Analog and Digital Circuits, Randall Geiger, Phillip Allen, Noel Strader, McGraw Hill Publishing co., 1990.
Planned learning activities and teaching methods:	Students are taught the course through lectures (3 hours per week) in classrooms or lectures theatres, by means of traditional tools or using computer demonstration. Auditory exercises, where examples regarding matter represented at the lectures, are solved and further, questions related to particular open-ended topic issues are compiled by the students and answered, during the lecture or assigned as homework. Topic notes are compiled by students, during the lecture which serve to cover the main issues under consideration and can also be downloaded from the lecturer's webpage. Students are also advised to use the subject's textbook or reference books for further reading and practice in solving related exercises. Tutorial problems are also submitted as homework and these are solved during lectures or privately during lecturer's office hours. Further literature search is encouraged by assigning students to identify a specific problem related to some issue, gather relevant scientific

	information about how others have addressed the problem and report this information in written or orally. Students are assessed continuously and their knowledge is checked through tests with their assessment weight, date and time being set at the beginning of the semester via the course outline. Students are prepared for final exam, by revision on the matter taught, problem solving and concept testing and are also trained to be able to deal with time constraints and revision timetable. The final assessment of the students is formative and summative and is assured to comply with the subject's expected learning outcomes and the quality of the course.
Assessment methods and criteria:	• Test1 (Static/ Dynamic Characteristics, Diode Logic): 20% • Test2 (CMOS Logic Gates): 20% • Final Exam: 60%
Language of instruction:	English
Work placement(s):	No