AEEE438 - VLSI Design

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<tr><td>Course Title</td><td colspan="5">VLSI Design</td></tr>
<tr><td>Course Code</td><td colspan="5">AEEE438</td></tr>
<tr><td>Course Type</td><td colspan="5">Technical Elective</td></tr>
<tr><td>Level</td><td colspan="5">BSc (Level 1)</td></tr>
<tr><td>Year / Semester</td><td colspan="5">3 / 1</td></tr>
<tr><td>Teacher's Name</td><td colspan="5">Dr. Konstantinos Tatas</td></tr>
<tr><td>ECTS</td><td>5</td><td>Lectures /week</td><td>2</td><td>Laboratories/ week</td><td>1</td></tr>
<tr><td>Course Purpose</td><td colspan="5">The aim of the course is to introduce students to VLSI design and optimization. Starting with transistor-level as well as layout-level design of common as well as custom cells, students learn to evaluate alternative designs in terms of speed, area and power consumption, using simple yet effective models. They are also introduced to simulation using SPICE as well as IC testing concepts such as fault modeling.</td></tr>
<tr><td>Learning outcomes</td><td colspan="5">1. Explain the function of nMOS an pMOS transistors.
2. Design the transistor-level schematic and layout of digital CMOS circuits.
3. Design CMOS VLSI circuits using a variety of EDA tools.
4. Optimize circuits for performance, area and power consumption
5. Describe the evolution of CMOS VLSI devices including 3D integration.
6. Predict the behaviour of CMOS devices and cells of a given technology node.</td></tr>
<tr><td>Prerequisites</td><td colspan="2">AEEE238</td><td>Co-requisites</td><td colspan="2">None</td></tr>
<tr><td>Course contents:</td><td colspan="5">• Introduction to CMOS Design: basic layout, subsystem layout, and mask layout, CAD/CAE tools. CMOS inverter, NOR and NAND gates.
• MOS Transistor Theory: Review of MOS transistor (nmos / pmos), current-voltage characteristics, capacitance. CMOS Inverter voltage transfer characteristics, noise margins, CMOS gate sizing, W/L aspect ratio.
• CMOS Processing Technology: Silicon Technology, Crystal growth through diffusion, ion implementation, oxidation, photolithography, metalization and packaging.
• Performance: circuit fan-out, logical and electrical effort. Logical effort and its application for transistor sizing. Optimal number of stages in a circuit.
• Power consumption: Static and dynamic power consumption component. Design for low-power consumptions. Performance/power trade-offs
• Simulation of CMOS Circuits using SPICE
• IC Testing: Fault modeling, SA-0 and SA-1 faults, scan registers, built-in-self-test
• More-than-Moore and Beyond Moore Technologies: 3D integration and alternatives to VLSI technology</td></tr>
<tr><td>Teaching Methodology</td><td colspan="5">The course is structured in lectures that are conducted with the help of both computer presentations and traditional means. Practical examples and exercises are included in the lectures to enhance the material learning process. Student questions are addressed during the lecture, or privately after</td></tr>
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	the lecture or during office hours. Open-ended questions are discussed in class or assigned as homework Lecture notes are available through the web for students to use in combination with the textbooks. Students are assessed continuously and their knowledge is checked through tests with their assessment weight, date and time being set at the beginning of the semester via the course outline. Furthermore, individual design assignments are used to develop practical engineering skills. Laboratory experiments are carried out in small groups and lab reports are required two weeks after the laboratory class resulting in a cumulative mark. The first laboratory exercises are totally structured (cookbook) in order to familiarize the students with the equipment, while later exercises are less structured, allowing the student to create and evaluate their own designs and solutions.
Bibliography	Textbooks: • Weste and Harris, CMOS VLSI Design: A Circuits and Systems Perspective, 4th edition, Addison Wesley, 2010. References • R. Baker, “CMOS Circuit Design, Layout, and Simulation”, 2nd edition, Wiley, 2007. • J. F. Wakerly, Digital Design: Principles and Practices and Xilinx 4.2i Student Package, Prentice Hall, 2003.
Assessment	The final assessment of the students is formative and summative and is assured to comply with the subject’s expected learning outcomes and the quality of the course. In order to continuously assess students, coursework weight is set at 40%, which comprises assignments, a mid-term exam and laboratory work assessment. Assignments range from simple problems to work out, to circuit design assignments that require demonstrate concept understanding as well as problem-solving skills. The assessment weight, date and time of each type of continuous assessment is being set at the beginning of the semester via the course outline. An indicative weighted continuous assessment of the course is shown below: • Assignments 10% • Tests: 10% • Laboratory Work: 20% • Final Exam: 60%
Language	English